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R. L. Sicotte

Design of Stable, High Efficiency, High Power Upper Sideband Upconverters

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Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts

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LINCOLN LABORATORY

DESIGN OF STABLE, HIGH EFFICIENCY, HIGH POWER UPPER SIDEBAND UPCONVERTERS

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Group 63

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ABSTRACT

This report presents a logical design procedure to build stable, efficient varactor-upper sideband upconverters. It establishes general design criteria to provide (1) unconditional stability, (2) low spurious, (3) predictable diode impedance levels, and (4) predictable efficiency. A sample design is included to illustrate one means of realizing the design constraints and showing the agreement between predicted and achieved stability, impedance match, efficiency, and power output.

The second part of the report discusses means of obtaining high power operation by using multiple varactors. It is concluded that the best configuration is a series stack of varactor diodes. With allowance made for the package parasitic reactances, it is proven analytically that stacked, packaged diodes operate efficiently as an upper sideband upconverter. Finally, an example of a stacked varactor upconverter design was built and measured. The agreement between predicted and obtained results is remarkably good.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

DESIGN OF STABLE, HIGH EFFICIENCY, HIGH POWER UPPER SIDEBAND UPCONVERTERS

I. INTRODUCTION

Three frequency upconverters have found extensive use in communications and radar systems. They provide the frequency translation and modulation capabilities required by these systems. For some systems, the upconverter is followed by power amplifiers in the transmitter section and has low power requirements. The design to be discussed was intended for use as the output stage of the transmitter section of an x-band communication system requiring it to handle power in the 10 watt range.

The purpose of this note is to present a logical approach for designing stable, high efficiency, three frequency upconverters capable of delivering up to 10 watts of power at x-band. The design impedance levels of the diode will be based on overdriven varactor upconverter theory established by Conning[1] at the three frequencies of interest. Design criteria will be presented to provide stability and suppression of harmonically related spurii.

Circuitry will be synthesized with the aid of microwave network analysis program to satisfy the design criteria. The final circuit will be measured and compared with the analyzed model. An efficiency analysis and performance results will be given.

The high power requirement is above the present single device capability. The performance of a stacked multiple chip device when used as an upconverter will be analyzed and compared with the performance of an experimental stacked varactor upconverter as a means to realize 10 watts of upper sideband power.

II. DESIGN REQUIREMENTS

A varactor diode is a non-linear device which can frequency multiply, mix, amplify and oscillate under certain loading and pumping conditions.

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[1] Reference 1

Consider the diode terminals removed from the operating circuit as shown in Fig. 1. In this section, a set of impedance requirements $Z(\omega)$ will be established to constrain the diode to operate as an upconverter only. This requires not only a conjugate match at the three frequencies of interest, but also constraints on the out of band impedance to prevent operation in an undesirable mode. From Conning[2], the impedance, power level and bias voltage (V_o) versus drive are calculated for a lossless diode normalized to $C_j \min = 1.0$ pf, $VB = 40V$ and $\gamma = 0$ (punch through diode capacitance law). The results are presented in Table I for the following design frequencies.

$$f \text{ signal} = 1.30 \text{ GHz}$$
$$f \text{ pump} = 6.0 \text{ GHz}$$
$$f \text{ USB} = 7.3 \text{ GHz}$$

Given the USB frequency, the pump and signal frequencies were chosen to ease the impedance matching problem and so that the harmonics of the signal frequency do not lie close to the other two frequencies of interest.

The varactor power and impedance levels are given by

$$P_k = K_p \upsilon (V_B^2) D_{min} \omega_k \tag{1}$$

$$Z_k = \frac{(K_r - jK_x)}{\upsilon C_{min} \omega_k} \tag{2}$$

where

$$\upsilon = \frac{1}{1 - \gamma} \tag{3}$$

is a function of the reverse bias diode capacitance law γ, and K_p, K_r and K_x are functions of the drive level $M \cdot M = 1$ corresponds to a diode fully driven, i.e., the total charge swings from 0 to Q_B the charge at the breakdown voltage. $M = 2$ corresponds the fully overdriven case, i.e., the total charge swings between $+Q_B$ and $-Q_B$. Table I together with (1) and (2)

2 Op. cit., 1.

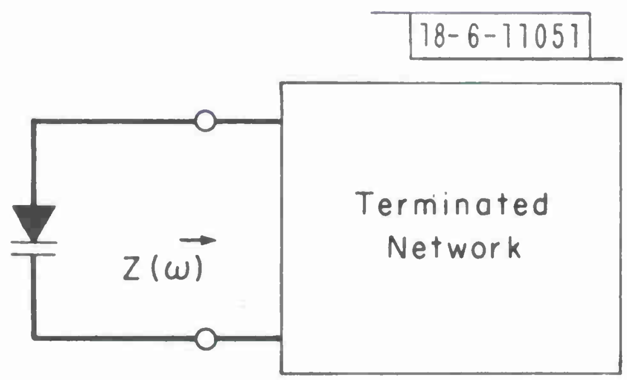

Fig. 1. Triplexer — diode Z(ω).

TABLE I

fs = 1.3 GHz
fp = 6.0 GHz
fUSB = 7.3 GHz

γ = 0
C_j min = 1.0 pf
VB = 40V

DRIVE	m = 1.5	m = 2.0	m = 2.5	m = 3.0
Rs Xs	15.5 −j108.8	26.0 −j62.2	21.55 −j23.9	14.32 −j11.95
Rp Xp	3.44 −j24.1	5.97 −j13.8	4.77 −j5.3	3.18 −j2.65
Ru Xu	2.83 −j19.83	4.91 −j11.34	3.92 −j4.36	2.61 −j2.18
Vo	11.20	6.80	2.40	0.80
P_s	.039w	.248w	.274w	.261w
P_p	.181w	1.15w	1.27w	1.21w
Pu	.220w	1.39w	1.54w	1.47w
Kp	.003	.019	.021	.020
K_R	0.13	0.255	0.180	0.120
Kx	0.910	0.52	0.20	0.10
K_v	0.28	0.17	0.06	0.02

enable the designer to scale impedance, power and bias voltage to any frequency, γ, V_B or C_j min .

In addition to the operating impedances of the diode at the three frequencies of interest, there are requirements on the out of band impedances presented to the diode. One of the most troublesome problems is stability, and the most common instability is due to parametric oscillation. Parametric oscillation arises from the negative resistance developed at some frequency f_1 when the diode is pumped at $f_3 > f_1$ and contains an idler current at $f_2 = f_3 - f_1$. The existence of the negative resistance is well documented[2, 3] and the magnitude can be readily predicted for small signal operation. Thus, the circuit will oscillate when the conditions of a sufficiently low loss idler at f_2 and a net negative real impedance exists in the diode circuit at f_1 .

One method proposed to solve the problem is to resistively load all frequencies below the pumping frequency to suppress idler currents and hence negative resistance. The method is sound until requirements for high efficiency are considered. For then it is necessary to effectively decouple these "lossy" branches from the diode at the operating frequencies. This requirement can complicate an initially simple design.

A better method is to reactively load the diode at all frequencies below the pump such that the diode is not resonated at possible idler frequencies thereby suppressing idler formation and negative resistance. This is the approach to be pursued here.

Finally, it is desirable to keep spurious harmonic and mixing product currents flowing through the diode at a minimum. The existence of large currents will lower efficiency and perturb the impedance calculations which are based on the fact that only the three currents of interest flow in the diode. The more important harmonically related spurious signals are listed in Table II. Suppression can be effected by placing a pole of impedance at the spurious frequencies. Since we are reactively loading at frequencies below the pump (f_p) a pair of poles say at 2fs and fp/2 will cause the reactance between them to vary between $\pm j \infty$ and will resonate the diode at some frequency between 2fs and fp/2 which is undesirable from stability considerations. Thus, instead of eliminating spurious current flow with poles of impedance, they will be

TABLE II

HARMONICALLY RELATED SPURII

Harmonic	Mixing Product
fs	fp − fs
2fs	fp + 2fs
fp/2	2fp + fs
3fs	
2fpλ	2(fp + fs)
3fp	

minimized by mismatching the impedance presented to the diode at those frequencies. Of prime importance is the suppression of the second harmonic currents of the three operating frequencies. Since higher order multiplier circuits require idler currents to flow for good efficiency, the suppression of the potentially strong second harmonics will reduce the amplitude of the higher order harmonics and the subsequent mixing product amplitudes.

From the above three considerations, i.e., (1) impedance matching, (2) stability requirements and (3) harmonic spurii suppression, it is possible to establish a $Z(\omega)$ characteristic for an upper sideband converter. This is shown in Fig. 2. $Z(\omega = 0) = 50$ ohms, the system characteristic impedance. It is desirable to start at either some real impedance or some highly capacitive impedance level at low frequencies to prevent possible low frequency oscillations due to the high probability of idler resonances close to the pumping frequencies fs and fp. $Z(\omega)$ then swings inductive to conjugate match the diode at fs. The pole of impedance between fs and fp is most advantageously placed between 2fs and fp/2, which lie close together in this design and thus suppress both these terms. $Z(\omega)$ remains capacitive (although several "loops"* may be encountered) up to fp at which point a conjugate match is presented to the diode. The characteristic will loop between fp and f_{USB} because of the fact that a larger inductive reactance is required at fp than at f_{USB} to resonate the diode average reactance. Finally, poles of impedance exist at 2fp and $2f_{USB}$ to suppress second harmonic spurii.

The basic three frequency upconverter circuit is the four port triplexer network shown in Fig. 3. It has the requirements of good frequency separation, efficient matching between the diode and Z_o, the rf system characteristic impedance. In addition, the impedance characteristic, $Z(\omega)$ looking into the diode terminals when the network is terminated in Z_o should closely approximate that given in Fig. 2 for best operation. A realization of such a circuit will be described in the following section for the frequencies of interest.

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* Resonances appear on a Smith Impedance Diagram as loops in the impedance vs frequency characteristic. Low loss resonant circuits have large loops and high loss circuits small loops. Thus resonances below the pumping frequency can be detrimental to stability if they are of sufficiently low loss to cause the $Z(\omega)$ characteristic to become inductive. See Ref. 5.

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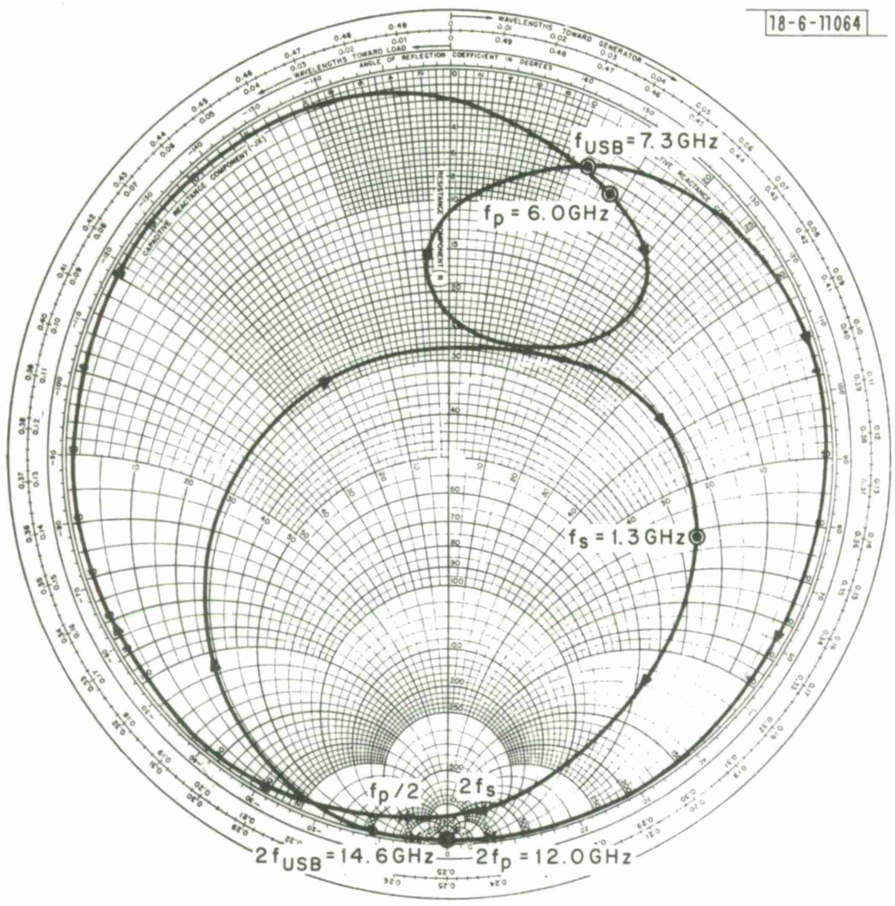

Fig. 2. $Z(\omega)$ characteristic plot (SMTCH).

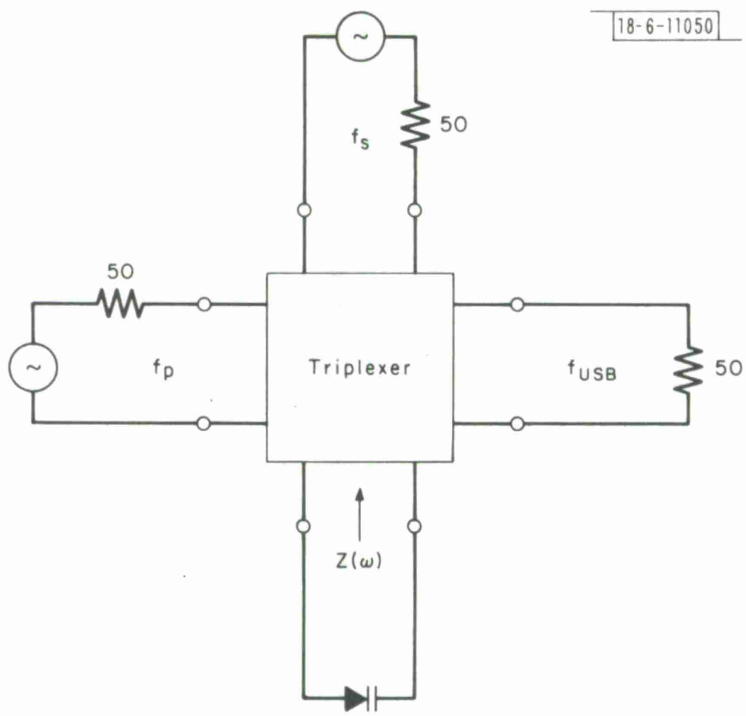

Fig. 3. Four port triplexer.

III. CIRCUIT DESIGN

The design Z_o for the system of interest is 50 ohms . Since the x-band circuits will handle the majority of the power, their losses are of prime interest. To check the design theory, it was decided to use bandstop filters* capacitively coupled to the diode at x-band because of their inherent simplicity and also the fact that they may be readily realized in low image impedance using relatively low loss circuit elements. The transmission line equivalent circuit of the triplexer is shown in Fig. 4. The circuit consists of four separate two port network branches. The branches labeled 1 through 4 are, respectively, the pump frequency bandstop filter and coupling network, the uppersideband frequency bandstop filter and coupling network, the signal low pass filter and signal return branch.

The functions of the four branches are as follows. The 6.0 GHz and 7.3 GHz bandstop filters form the x-band diplexer network to match the diode at the two frequencies and separate the pump and upper sideband signals, the pump power being transferred through the 7.3 GHz BSF and the USB power through the 60 GHz BSF . The filters are designed for $Z_o = 10\Omega$ with an impedance to 5Ω† . The series open circuit stub lines provide capacitive coupling required to resonate the packaged diode equivalent series reactance at each respective x-band frequency and also decouple the signal power from the x-band arms. The signal low pass filter has a characteristic impedance equal to the real part of the diode impedance at 1.3 GHz , the signal frequency. It provides some series capacitance at x-band to help resonate the diode. The importance of this capacitance will be considered in Section IV for efficiency optimization. The filter effectively decouples the x-band signals from the signal arm. The signal return branch is comprised of two series quarter

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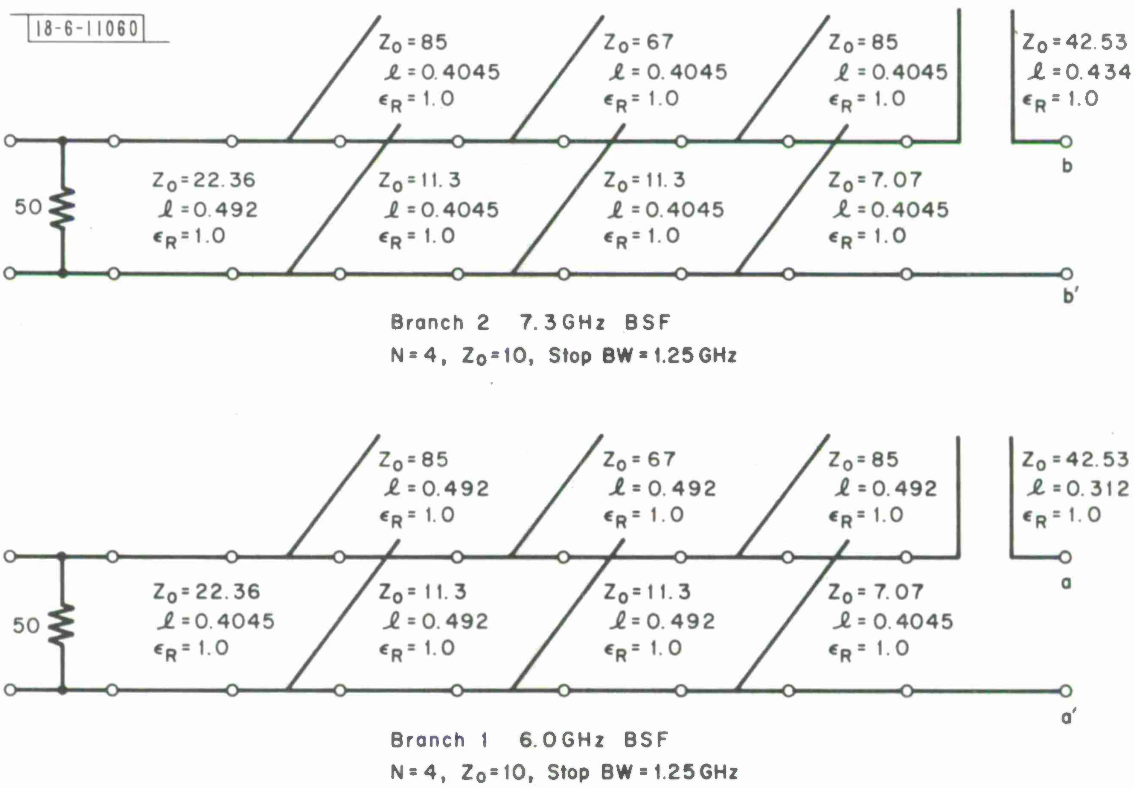
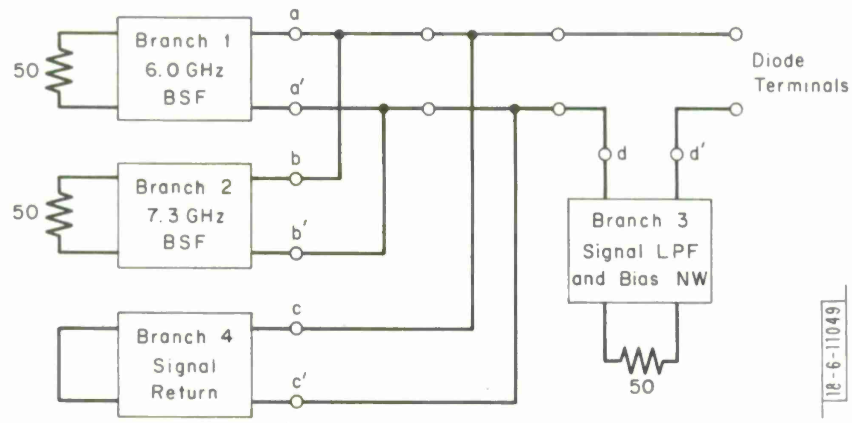
* Triplexer synthesis is not limited to bandstop filter triplexers. Triplexers have been designed using low pass and high pass filter combinations and also bandpass filter combinations which satisfy the design requirements and have certain advantages and disadvantages when compared to the bandstop filter designs. The bandstop filter design is used here for illustration.

† See Appendix for the effects of diode package parasitics. It was subsequently found that the packaged diode was more closely matched by making $Z_t = 10\Omega$.



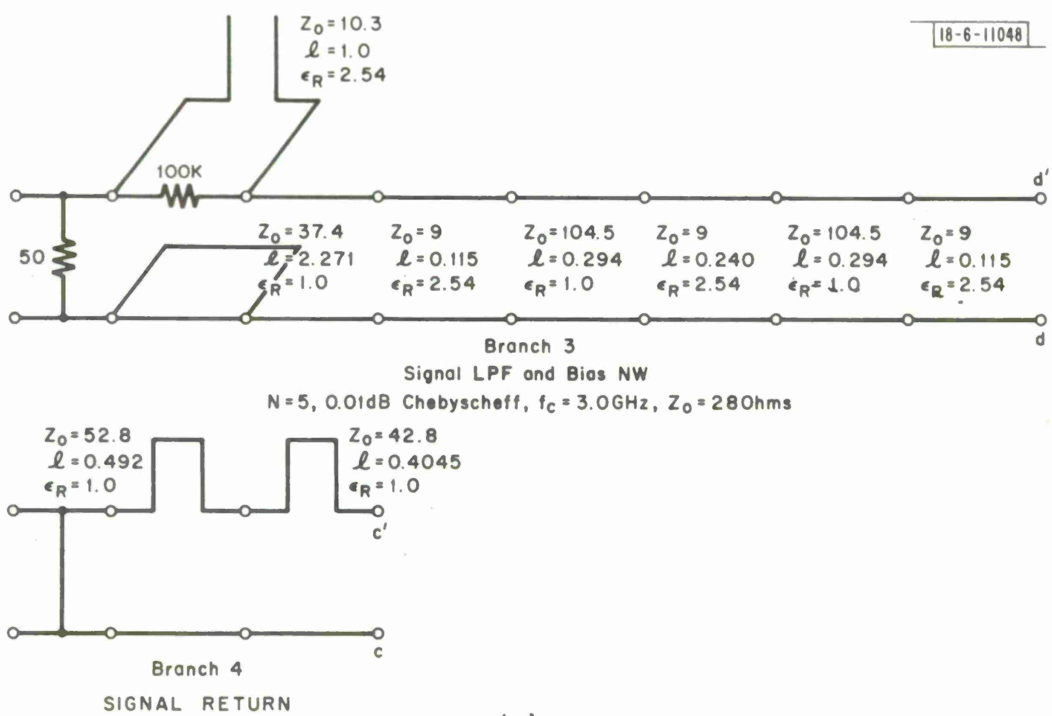
(a)

Fig. 4. Microwave network analysis circuit.



(b)

Fig. 4. Continued.



(c)

Fig. 4. Continued.

wavelength short circuited transmission lines. One is a quarter wavelength at the pump frequency and the other at the USB frequency. Their characteristic impedances are chosen to resonate the average reactance of the diode at the signal frequency.

The circuit was analyzed with the aid of an automatic microwave network analysis computer program[6] for driving point impedance at the diode terminals and transmission loss characteristics through branches 01, 02 and 03. The configuration of Fig. 4 was arrived at by designing and analyzing each branch separately then assembling them as shown and making final changes with several iterations of design and analysis. This design procedure enables one to quickly evaluate the branch interactions and make the necessary modifications to arrive at the desired $Z(\omega)$ characteristic. The final computer generated impedance plots looking into the diode terminals are presented in Figs. 5 and 6 for frequencies between DC and 15 GHz. Each arm is decoupled from the other two by at least 30 db at the three frequencies of interest. This circuit was constructed in coaxial form using the split block technique and is shown pictured in Fig. 7. Fig. 8 shows a plot of the measured impedance presented to the diode by the triplexer of Fig. 7 from 110 MHz to 8 GHz. The differences between the calculated and measured impedances are due to the parasitic reactances about the junction of the four branches. The differences were considered minor and no attempt was made to modify the analysis circuit for the parasitics.

Along with a design for stability, impedance matching and spurii minimization, the circuit was optimized for efficiency.

Consider the finite Q diode in operation as a frequency conversion device. The diagram of Fig. 9 shows the lossy R_S in series with some R which results when power is transferred from branch 1 to branch 2. The percentage of the input power delivered to R_1 (that converted) is a simple function of R_s and R_1, i.e.,

$$\frac{P_{R_1}}{Pin} = \frac{R_1}{R_1 + R_s} \tag{4}$$

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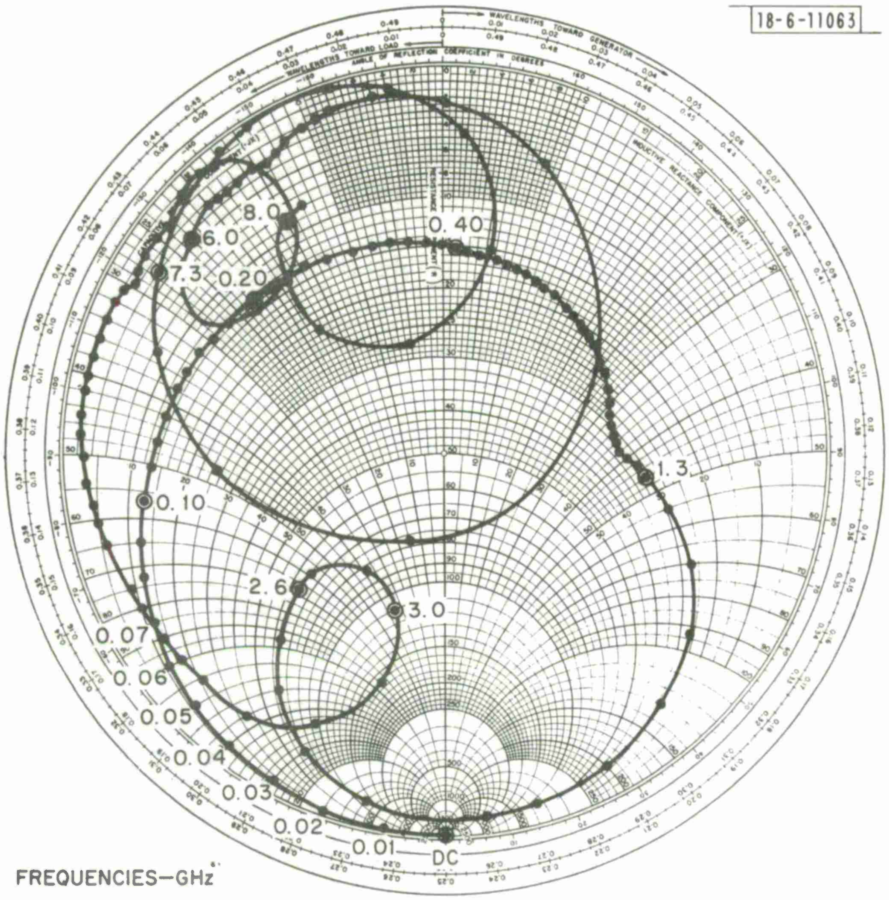

Fig. 5. $Z(\omega)$ characteristic plot – GCP.

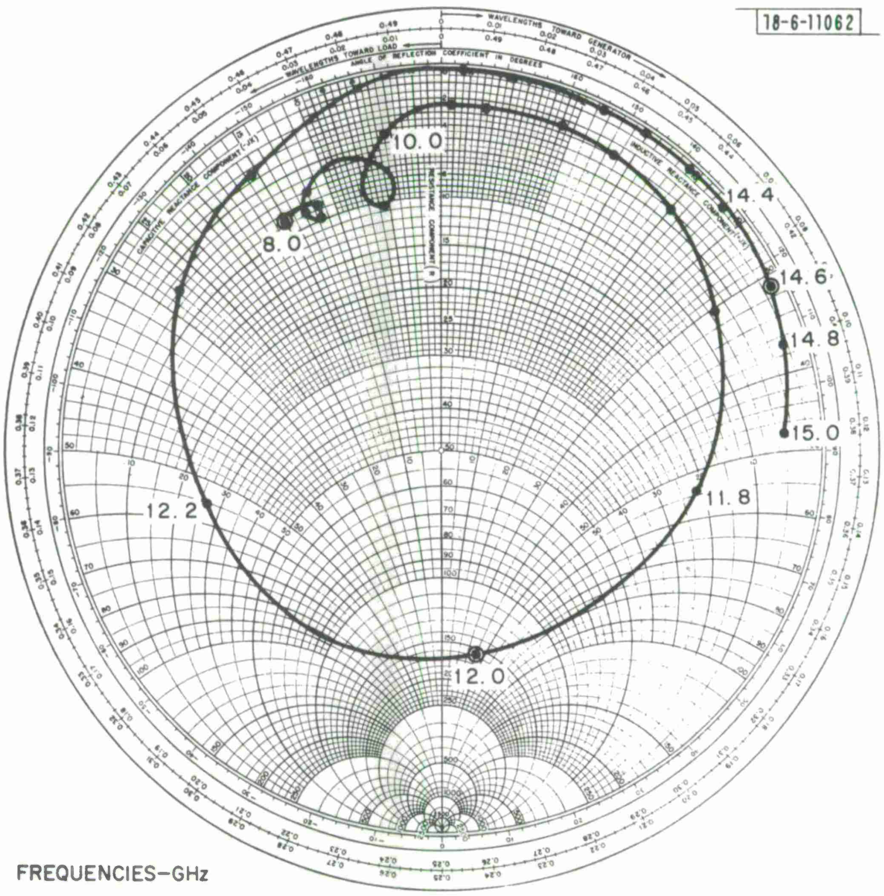

Fig. 6. Z(ω) characteristic plot – GCP.

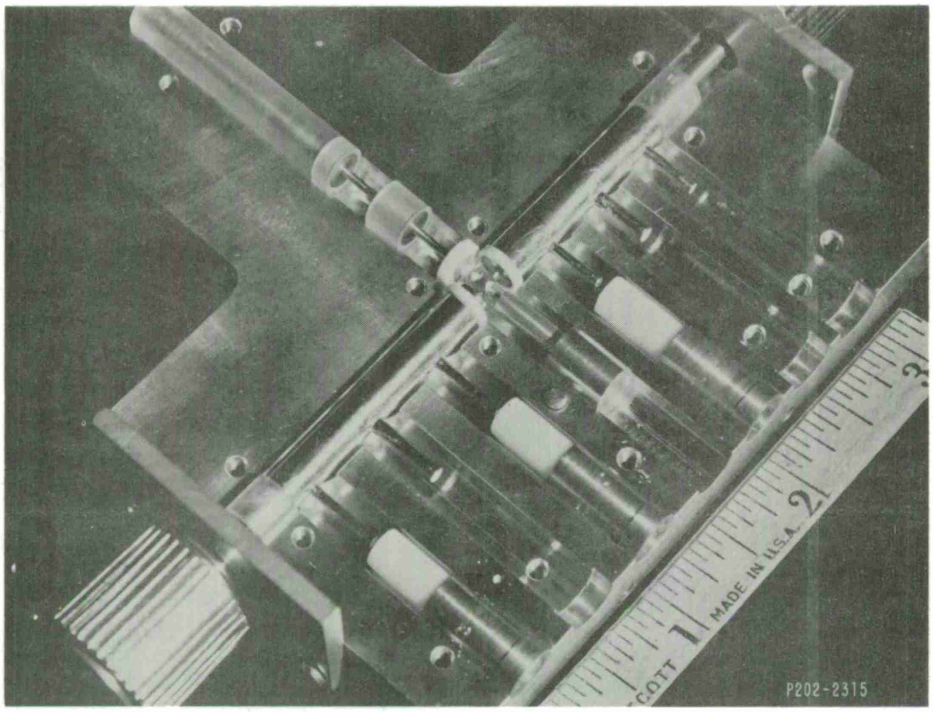

Fig. 7. Coaxial USBUC picture.

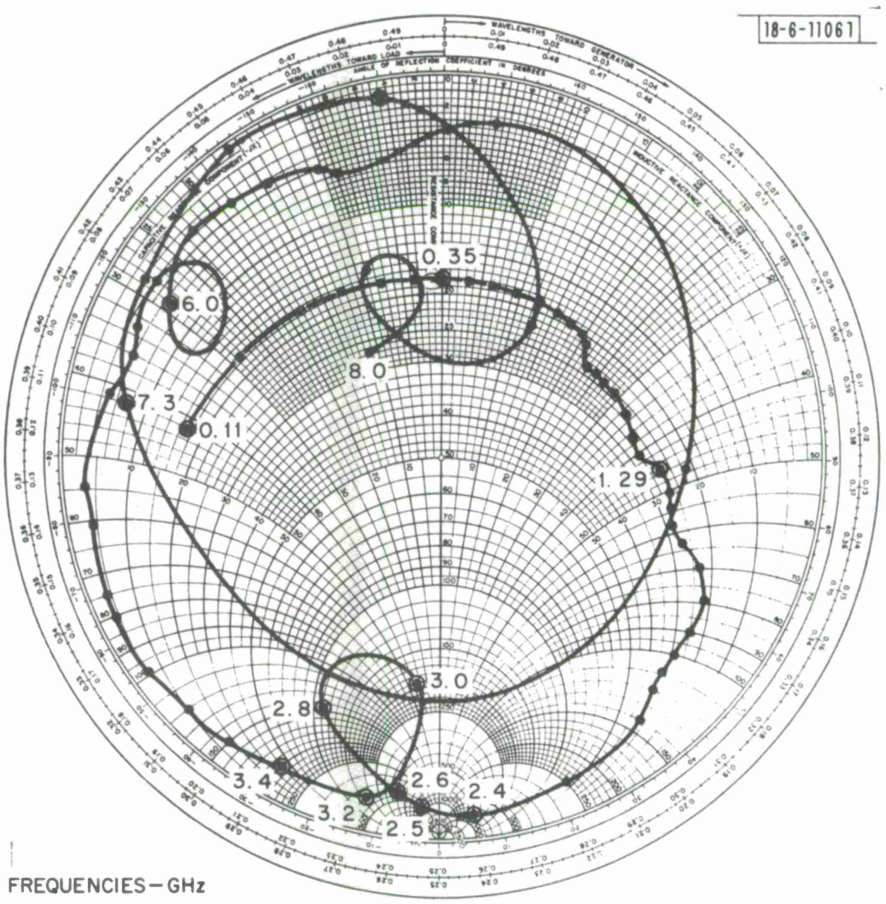

Fig. 8. $Z(\omega)$ characteristic plot – measured.

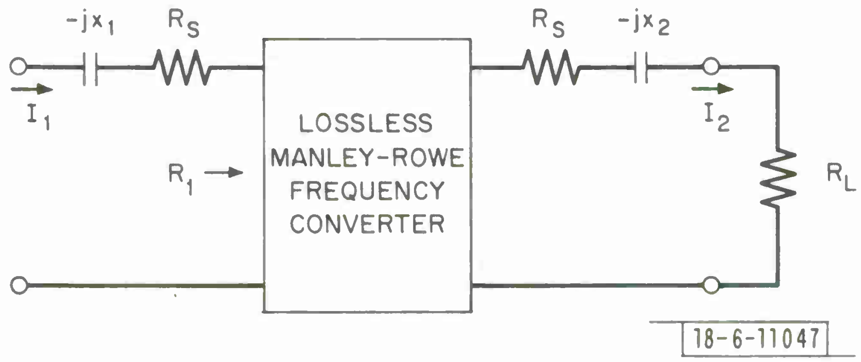

Fig. 9. Conversion loss equivalent circuit.

Since R_1 is related to $\omega_1 C_{min}$, M, and γ, the efficiency can be related to diode Q, drive level and capacitance law. Usually R_s denotes the bulk resistance of the semiconductor. However, the circuit resistances in series and in shunt effectively load the Q of the diode such that the theoretical maximum efficiency for finite Q diodes can only be approached.

For the circuit considered here, the diode is in shunt with the x-band diplexer and in series with the signal low pass filter. The equivalent circuit for purposes of efficiency analysis can be represented at x-band by that of Fig. 10.

The ratio of power transferred to RD the conversion resistance of the pumped diode to the power delivered to the circuit is

$$\eta_1 = \frac{R_p R_{SH}}{R_{SH}(R_p + R_s + R_F) + (R_s + R_F + R_p)^2 + |X_p - X_F|^2} \qquad (5a)$$

Similarly, the ratio of power delivered to the optimum load resistance R_L to that converted at the uppersideband is

$$\eta_2 = \frac{R_L R_{SH}^2}{R_L^2(R_s + R_F + R_{SH}) + R_L[2R_{SH}(R_s + R_F) + R_{SH}^2] + (R_S + R_F)R_{SH}^2} \qquad (5b)$$

Equations (5a) and (5b) are derived from (6a) and (6b), respectively, with reference to Fig. 10.

$$\eta_1 = \frac{P_{conv}}{P_{loss_p} + P_{conv}} \qquad (6a)$$

$$\eta_2 = \frac{P_{load}}{P_{loss_u} + P_{load}} \qquad (6b)$$

The pump efficiency is given by the product of the efficiencies of the pump

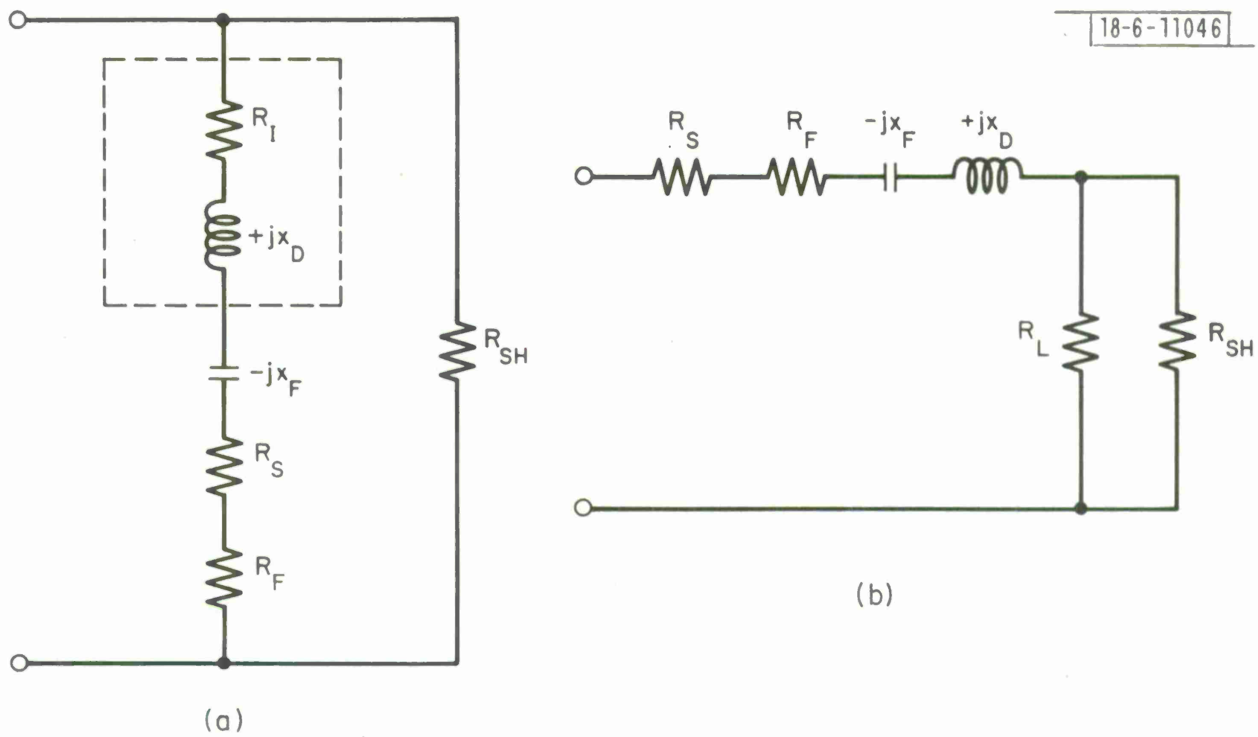

Fig. 10. Efficiency equivalent circuit.

and USB branches.

$$\eta_p = \eta_1 \cdot \eta_2 \quad . \tag{7}$$

R_{SH} — shunt resistance presented by open circuited x-band branch

R_F — series loss resistance of LPF

R_p — conversion loss resistance of the diode at the pump frequency referred to the package terminals

X_p — net reactance in series with R due to package parasitics and average junction reactance at the pump frequency

X_F — the series reactance (capacitive) of the LPF at pump frequency

R_s — series loss resistance of the diode referred to the package terminals

P_{loss_p} — power dissipated (loss) in the pump circuit

P_{loss_u} — power dissipated (loss) in the USB circuit

P_{conv} — pump power converted to the USB circuit

P_{load} — power delivered to the optimum R_L at the USB frequency

It is important to minimize the quantity $|X_D - X_F|$ at the pump frequency to optimize efficiency. This is evident from equation (5a). The theoretical pump efficiency for a diode having $R_S = 0.79\Omega$ and $C_{j\,min} = 1$ pf is shown plotted for the frequencies of interest in Fig. 11.

The circuit branches were designed to maximize R_{SH} and minimize R_F. The minimization of R_F was accomplished using low loss dielectric material, copper plating the elements 3 skin depths thick at x-band and gold flashing the signal low pass filter. The impedances of the shunt stubs used in the bandstop filters were chosen close to the lowest loss 76Ω level. Then the number of sections was determined by the maximum allowable rejection bandwidth and finally the entire assembly was copper plated 3 skin depths thick at the x-band frequencies and gold flashed. The final measurement of the filters

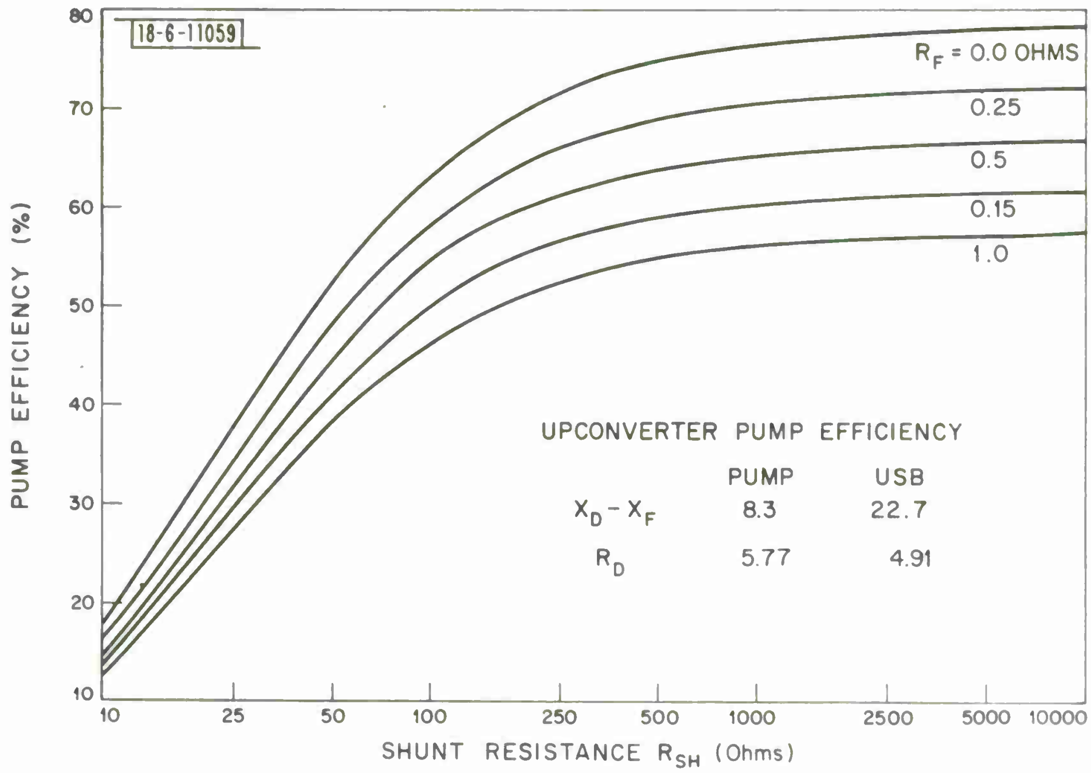

Fig. 11. Efficiency plot.

TABLE III

SINGLE CHIP OPERATING IMPEDANCES

					Junction Impedances						Package Diode Impedances					
					Z_s		Z_p		Z_u		Z_s		Z_p		Z_u	
P_{pump}	P_{in} Sig	P_{usb}	n_p	n_t	R_s	X_s	R_p	X_p	R_u	X_u	R_s	X_s	R_p	X_p	R_u	X_u
2.0 w	500 mw	980 mw	49.1	39	28.65	−j38.19	6.4	−j12.1	7.2	−j19.1	26.4	−j30.6	8.5	+j24.7	10.2	+j25.9
	400	920	46	38.3	27.32	−j38.1	6.9	−j12.6	7.2	−j18.5	25.2	−j30.4	9.1	+j24.1	10.3	+j26.7
	300	840	42	36.5	18.3	−j45.4	5.2	−j14.1	7.7	−j18.5	16.6	−j36.7	6.7	+j22.3	11.0	+j26.7
	100	340	17	16.2	19.1	−j43.5	4.9	−j12.7	9.3	−j23.1	17.4	−j35.0	6.5	+j24.2	12.3	+j20
1.5	420	770	51.3	40.1	21.2	−j43.8	7.5	−j14.0	6.3	−j20.3	19.3	−j35.3	4.6	+j22.2	8.7	+j24.4
	300	730	48.7	40.6	16.6	−j48.7	7.1	−j16.0	6.3	−j20.9	14.9	−j39.5	8.9	+j19.7	8.7	+j23.5
	200	610	40.7	35.9	18.7	−j50	5.7	−j17.5	9.2	−j21.3	16.8	−j40.8	7.0	+j17.9	12.6	+j22.4
	100	330	22	20.6	22.6	−j46.8	3.5	−j16.1	10.6	−j20.7	20.5	−j38.1	4.5	+j19.8	14.6	+j22.9
1.0	400	540	54	38.6	17.12	−j47.0	8.0	−j14.0	8.2	−j20.8	15.5	−j38.0	10.3	+j22.1	11.3	+j23.3
	300	530	53	40.26	15.6	−j52.2	8.8	−j17.2	7.0	−j20.3	13.9	−j42.6	10.9	+j17.8	9.7	+j24.3
	200	500	50	41.7	15.2	−j58.3	7.3	−j15.9	6.3	−j22.1	13.4	−j48.0	9.2	+j19.7	8.5	+j21.9
	100	310	31	28.2	25.0	−j59.3	3.9	−j18.6	7.8	−j23.2	21.9	−j49.3	4.8	+j16.8	10.4	+j20.2
0.75	400	420	56	36.5	16.5	−j49.0	3.9	−j18.6	6.8	−j21.4	14.9	−j39.8	4.8	+j16.8	9.3	+j22.7
	300	410	54.7	39	15.6	−j51.8	5.9	−j15.5	7.7	−j20.2	13.9	−j42.2	7.6	+j20.4	10.7	+j24.2
	200	390	52	41.1	15.6	−j61.2	5.1	−j16.6	7.3	−j22.6	13.6	−j50.6	6.4	+j19.2	9.8	+j21.0
	100	290	38.7	34.1	17.5	−j67.3	4.1	−j16.6	6.6	−j22.1	15.0	−j55.9	5.1	+j19.2	8.9	+j21.9
	50	150	20	18.8	16.7	−j65.56	3.6	−j17.7	8.3	−j22.6	14.4	−j54.4	4.4	+j17.9	11.1	+j20.9
0.5	300	260	52	32.5	15.4	−j53.6	6.3	−j15.0	8.0	−j22	13.1	−j48.9	8.0	+j21.0	10.8	+j21.7
	200	260	52	37.1	15.5	−j61.1	7.7	−j16.9	5.9	−j23.9	13.5	−j50.5	9.5	+j18.5	7.8	+j19.5
	100	210	42	35	18.5	−j69.9	5.2	−j17.6	6.4	−j23.9	15.8	−j52.2	6.3	+j17.9	8.4	+j19.5
	50	140	28	25.5	20.1	−j71.5	4.1	−j17.6	5.9	−j23.9	17.11	−j59.6	5.1	+j17.9	7.8	+j19.5

gave $R_{SH} \approx 1000\Omega$ and a corresponding theoretical pump efficiency of 70% ($R_F = .25\Omega$). The efficiency does not take into consideration the filter losses; they are estimated to degrade the quoted efficiency by less than 5%.

IV. UPCONVERTER OPERATION

The upconverter was operated using a silicon punch through varactor diode having the following manufacturer quoted characteristics:

$$C_j(-6) = 1.07 \text{ pf}$$

$$V_B(10\ \mu a) = 45v$$

$$f_c(-6) = 169 \text{ GHz}$$

$$\text{Punch Through Voltage (PTV)} \approx 6v$$

The diode packaged in a standard pill-prong microwave diode package (described in the appendix) was operated in the triplexer circuit both with fixed and self (resistive) bias. The circuit delivered 1.12 watts maximum under fixed bias conditions, however, a net current of 2 ma was flowing in the avalanche direction.

Pump efficiencies of up to 67% were measured at the 1 watt output level, which is comparable to that calculated in section III.

The circuit was stable for all combinations of pump and signal power levels. To check stability, analog power plots were taken from the power meters and are shown in Fig. 12. Abrupt changes in power level (glitches) usually indicate instabilities. The plots are smooth and resemble the familiar amplifier characteristic showing various levels of saturation for various pump drive levels.

Another experiment involved tuning the upconverter externally at a number of power levels by means of sliding slug tuners. The diode was then removed and the impedances presented to the diode from each side (1) measured for each combination of setting corresponding to an operating point, and (2) added to give the circuit impedance presented to the diode at the package terminals. The complex conjugate of this impedance is listed in Table III as

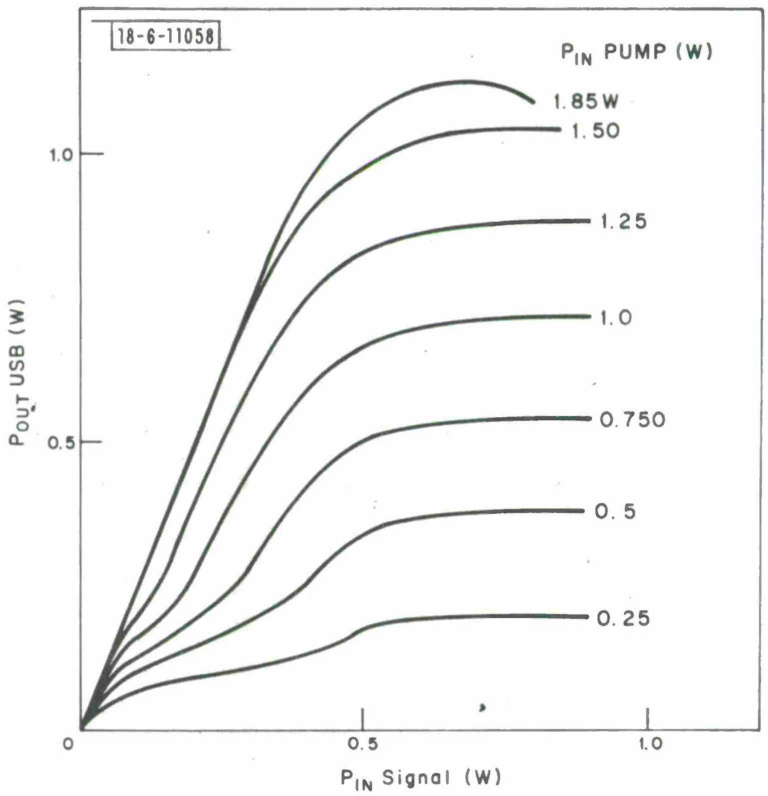

Fig. 12. Power performance curves.

the packaged diode impedances. A simple transformation (see appendix) was performed to find the junction impedance. The impedances are seen to predict rather closely particularly in view of the fact that the varactor is not on ideal punch through device and that the package transformation is approximate.

Harmonically related spurii were present at the three ports. The strongest measured at the output port are shown in Table IV below. No attempt has been made to reduce their level at the output.

TABLE IV

SPURIOUS LEVELS

Spurious	Frequency	Level*
fs	1.3 GHz	– 26 db
2fs	2.6	– 20.7 db
fp-fs	4.7	– 33 db
fp	6.0	– 50 db
2fs + fp	8.6	– 20 db
2fp	12.0	– 31.5 db
2(fp + fs)	14.6	– 58 db
3fp	18.0	– 45 db

It is important to note that the predicted impedance characteristic of the circuit shown in Fig. 5 shows a potentially unstable region at frequencies just below the pump as the impedance characteristic swings inductive (when viewed at the diode junction). The negative resistance will occur at some low (< 100 MHz) frequency. This fact places constraints on the bias circuit design. The bias decoupling (D. C. block) should be placed as close to the diode junction as possible to insure stability.

V. HIGH POWER UPCONVERTERS

The power handling capability of a varactor diode at a given frequency is proportional to υC_{min} $(V_B{}^2)$ and the impedance level consistent with $\frac{1}{\upsilon C_{min}}$. It is necessary to fix a minimum impedance level consitent with good power

* Referenced to USB output power level.

transfer efficiency. Operation in a 50Ω system requires low impedance transformers and low impedance filters to match the low real part of the diode impedance. The lower the diode impedance, the more lossy the filters and transformers become and hence the poorer the efficiency. Also, many filters become very difficult to realize in low image impedances. For these reasons, an arbitrary level of 50Ω is set for the minimum diode impedance level consistent with efficient matching. This corresponds to the real part of the diode impedance at 7.3 GHz for a C min = 1.0 pf , υ = 1 varactor. Diodes are available with capacitances up to 3 pf at the same breakdown voltage and Q of the 1 pf devices.

The 1 pf , υ = 1 device with a state-of-the-art breakdown voltage of 45 V will theoretically handle 1.95 watts maximum at 7.3 GHz . The equivalent Q 3 pf device could handle only three times this amount but has 1/3 the impedance of the 1 pf device. The matching network becomes more lossy which leaves doubt about the 3 pf circuit delivering three times the power. Clearly some means of combining power from multiple chips is required. Two will be explored; (1) stacking single chip circuits and (2) stacking chips in one circuit.

To deliver a theoretical 10 watts using the 1 pf device would require 5-plus circuits because in stacking circuits, the power goes up as N , the number of devices (circuits). However, by series stacking devices, while maintaining a constant impedance (overall capacitance), the power level goes up as $(N)^2$ assuming each chip has the same breakdown voltage, and the matching efficiency is as good as for the 1 chip, 1 pf device. Thus a series stacking of three 3 pf devices gives an overall C_j min = 1 pf and $V_{B'} = 3V_B$ and a power handling capability of

$$9 \times 1.95 = 17.55 \text{ watts}$$

at 7.30 GHz . The stacked device can be imbedded in the single chip circuit and run at comparable efficiency if the chips are properly stacked electrically. Clearly there is an advantage of series combining devices over combining circuits when the lower impedance devices are available.

Parallel connection of chips is not desirable for two reasons. (1) Higher power is achieved at the expense of lower impedance and not of higher impedance. Since higher impedance chips are desirable for parallel stacking, that stacking concept is incompatible with high power operation. (2) Invariably, parasitic inductances are encountered between the chips. The parallel stacking along with the parasitic interconnecting inductances can cause loop resonances or low impedance idler circuits and stability problems.

Proposals have been advanced recently to stack (series or parallel) varactor packages separated by line lengths $n\lambda/2$ long. This method of stacking does have power dissipation advantages over the stacked varactor package but suffers from the three disadvantages: narrower stability margin, inflexible frequency selection, and narrow bandwidth, The interconnecting lines must be carefully designed in conjunction with the triplexer circuit to guarantee stability, i.e., a circuit which is stable for a single chip device is not necessarily stable for the $n\lambda/2$ stacked devices. The three frequencies are limited to being commensurate to make the interconnecting line $n\lambda/2$ long at each frequency. The bandwidth is limited by the fact that the electrical length of the interconnecting lines is a function of frequency.

There are three major problems encountered in series stacking varactor chips in a package. They are: (1) heat removal, (2) stacking efficiency, i.e., how much of the ideal series chip power is available when interconnecting parasitics are present and (3) diode impedance transformations due to the package. The first two items are explored below and the effect of the last item is reflected in the diode impedance measurements of Tables VI and VII of Section V-C.

A. Thermal Performance

Consider the commercially available package in Fig. 13 for three series stacked chips. It ismade up of sections of BEO rings and Tellurium Copper metallic contacts. The diodes are mounted on the three pedastels and connected to the upper package module by the bonded strap. The thermal equivalent circuit (electrical analog) is shown in Fig. 14, where the resistors

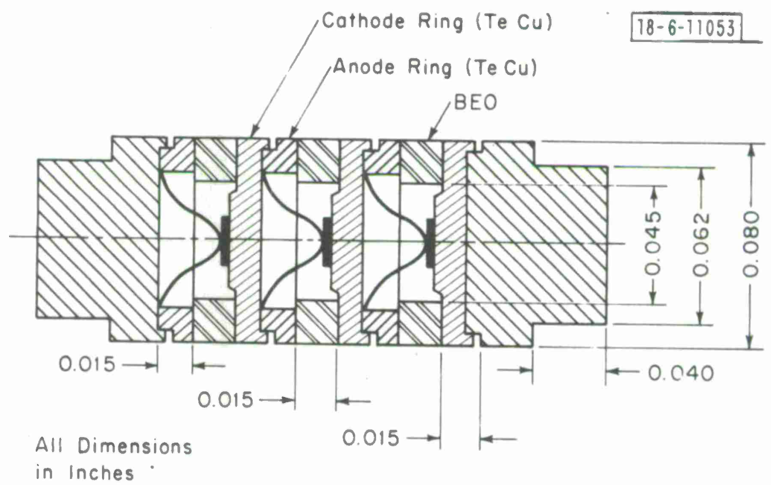

Fig. 13. Stacked package.

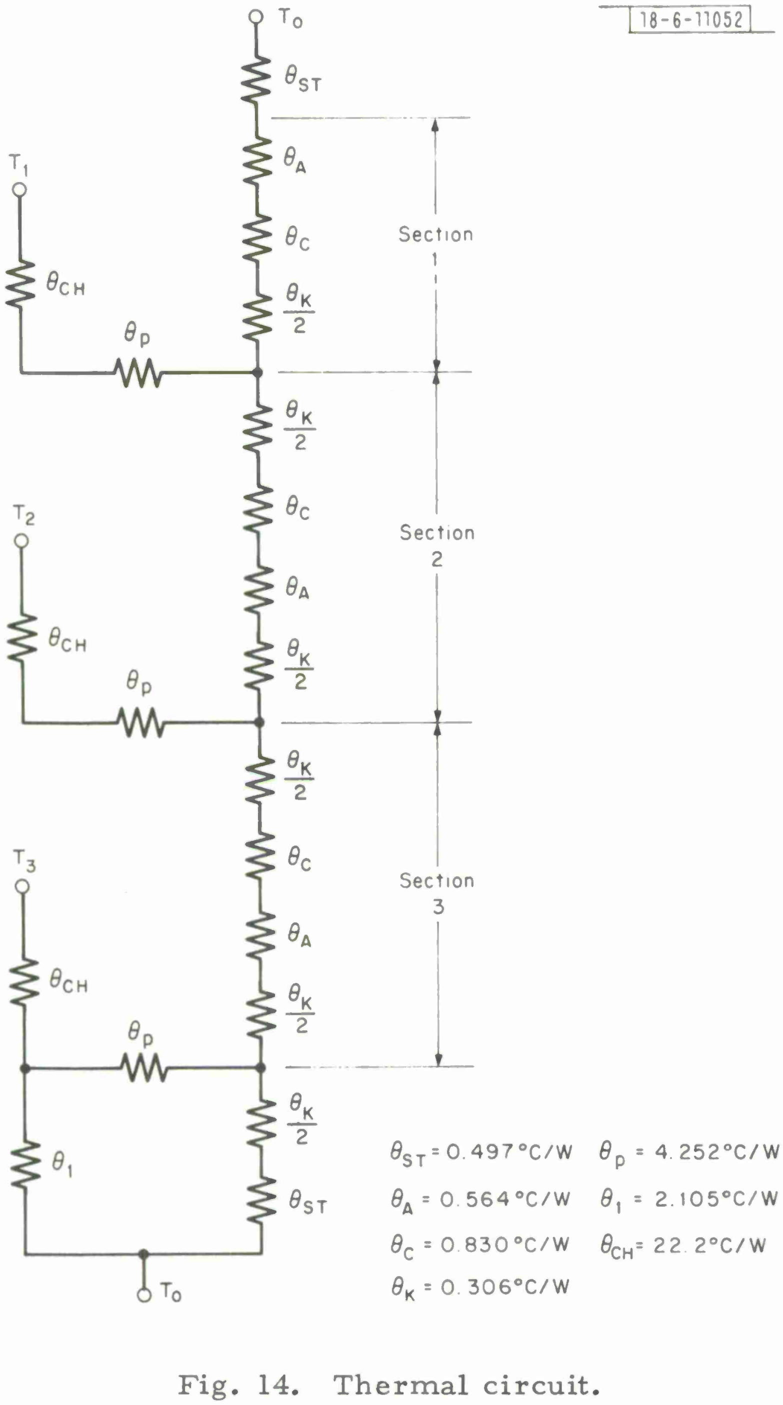

Fig. 14. Thermal circuit.

represent thermal drops in $^{o}C/\omega$ as noted. These are readily calculated given the thermal conductivities and geometrical shape of the conductors. The circuit is solved using mesh equations and determinants. The resulting temperature drops between the chips and end caps for a package with heat sinks on both ends are:

$$\theta_j\ 1-0 = 27.36^{o}C/\omega$$

$$\theta_j\ 2-0 = 27.33^{o}C/\omega$$

$$\theta_j\ 3-0 = 23.61^{o}C/\omega$$

which compare favorably with the $23^{o}C/\omega$ temperature drop for the same chip in a conventional pill-prong microwave diode package. For a T_o (the heat sink temperature) of $20^{o}C$ and a diode upper operating temperature of $175^{o}C$ (silicon) the allowable power dissipation per chip is 5.67 watts for the hottest running chip or $3 \times 5.67\ \omega = 17\ \omega$ for the entire package. This is an upper dissipation limit. For a circuit to operate at 40% efficiency and deliver 10 watts, 15 watts will be dissipated in the circuit of which 8 – 12 watts is dissipated in the diode junction. Clearly the package will do the job thermally.

B. Electrical Performance

To analyze the problem, it is assumed that a series string of pumped varactor diodes separated by linear, passive, lossless networks is operating an an upper sideband upconverter. The procedure involves analyzing the distribution of pump and signal power per diode and the percentage of upper sideband power delivered to a matched load (compared to that for an equal number of chips in exact series) at the diode package terminals. A pumped lossless diode has the equivalent circuit shown in Fig. 15. R and X are functions of the pumping frequency f, the minimum junction capacitance C min, γ the diode law, and M the drive level. R represents the power loss at f due to the conversion process only. Thus in analyzing the electrical phase between

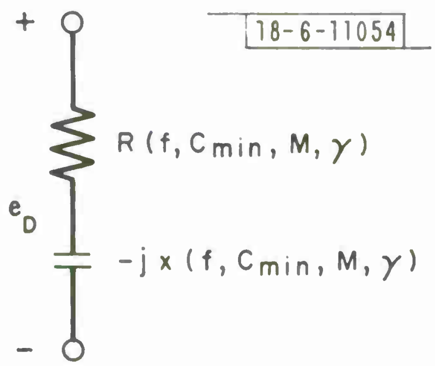

Fig. 15. Pumped lossless diode — equivalent circuit.

pumped varactors, the phase and amplitude of the voltage across R is of interest and $-jX$ is absorbed into the two port interconnecting network as shown in Fig. 16.

It is possible to describe the network using generalized ABCD matrices as defined in Fig. 17.

$$V_1 = AV_2 - BI_2 \tag{8}$$

$$I_1 = CV_2 - DI_2 \tag{9}$$

At the output frequency, the diodes are considered as generators with an internal impedance $Ru - jX$. The power at the USB frequency is given by the Manley-Rowe relationships

$$\frac{Pu}{Pp} = \frac{fu}{fp} \tag{10}$$

$$\frac{Pu}{Ps} = \frac{fu}{fs} \tag{11}$$

and for a lossless upconverter

$$Pu = P_p + P_s \tag{12}$$

Pu is the power delivered to a matched load and Eu is the voltage across that load. Thus $Pu = Eu \cdot Iu$ (12). The equivalalent generator is shown in Fig. 18* and has a maximum available power given by

$$(P_{AVAIL})\ USB = \frac{|Eu|^2}{Ru} = Pu \tag{13}$$

* The generator is so defined to make the maximum available power equal to P_u, the Manley-Rowe power delivered to the matched load.

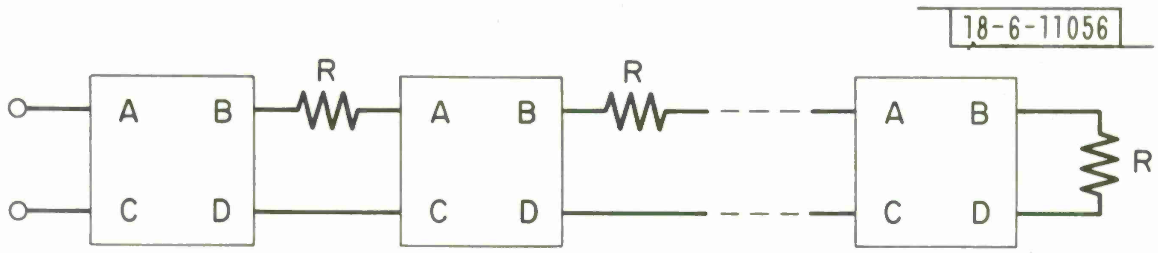

Fig. 16. Series pumped varactors with interconnecting networks.

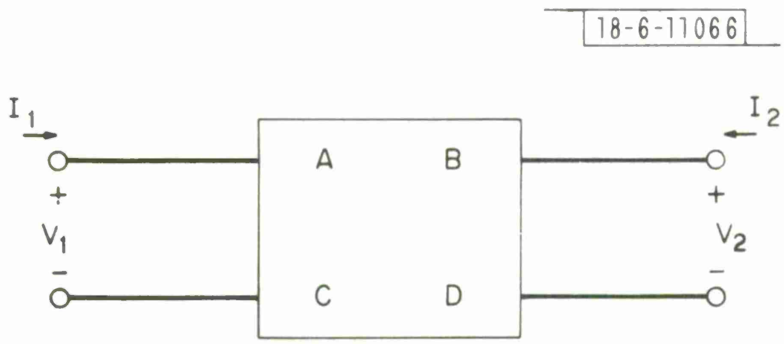

Fig. 17. ABCD matrix.

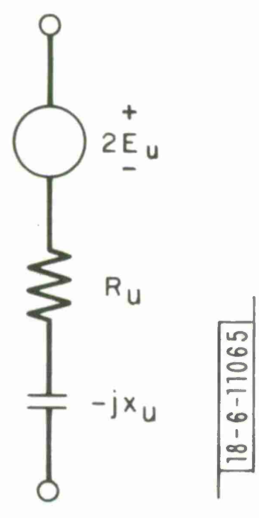

Fig. 18. Diode equivalent circuit at USB.

Defining VDS as the voltage across the pumped diode resistance Rs at the signal frequency and VDP across Rp at the pump frequency, and from (11)

$$\frac{|Eu|^2}{Ru} = \frac{|VDS|^2}{Rs} + \frac{|VDP|^2}{Rp} \quad . \tag{14}$$

From (2), the R_k are inversely proportional to ω_k , i. e. , $\frac{Ru}{Rs} = \frac{fs}{fu}$ and $\frac{Ru}{Rp} = \frac{fp}{fu}$ and (13) becomes

$$|Eu| = \left(|VDS|^2 \frac{fs}{fu} + |VDP|^2 \frac{fp}{fu}\right)^{\frac{1}{2}} \tag{15}$$

The phase of Eu is given by

$$\underline{|Eu} = \underline{|VDP} + \underline{|VDS} \tag{16}$$

The varactor impedance levels are calculated from (1) and (2) in Section II.

A computer program was written to calculate the phase and amplitude of Vs, Vp and Eu and hence the power distribution in the varactors at fs and fp and fu . Finally the power delivered to a matched termination at fu was calculated at each end of the array. This was accomplished by short circuiting the end where fp and fs enter at fu and calculating the equivalent generator and hence power available at fu at the end where fp and fs enter, the opposite end being short circuited at all three frequencies. The differences between the two cases were minor for this particular diode.

An approximate electrical equivalent circuit of the package is shown in Fig. 19.

For good performance, C_j min was chosen to be ten times C_c . In operation, the average junction capacitance is greater than C min and the magnitude of the diode impedance plus the series inductive reactance associated with the strap (short section of transmission line inside the loop contain-

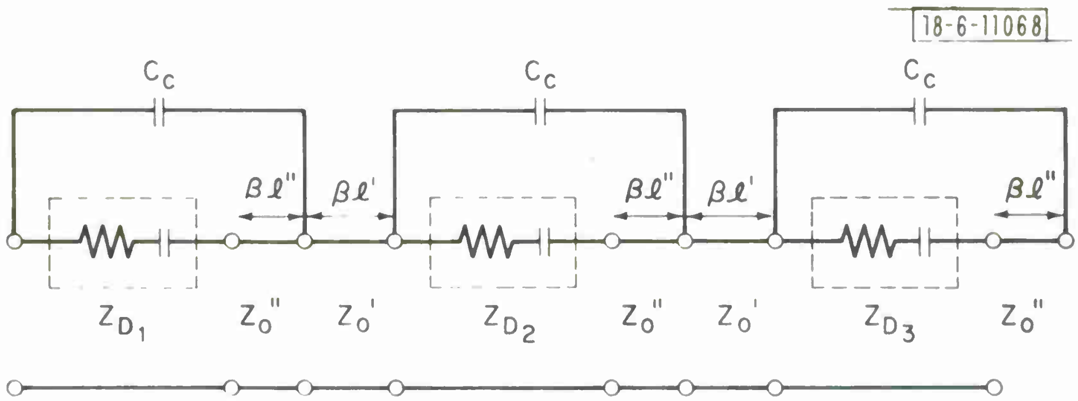

Fig. 19. Electrical equivalent circuit — stacked diodes.

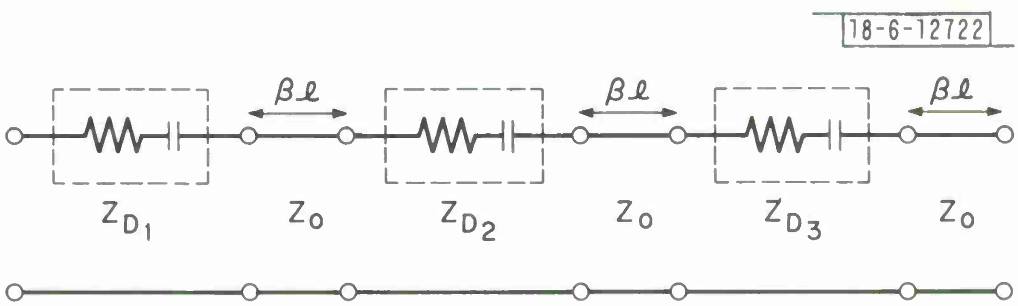

Fig. 20. Simplified equivalent circuit.

ing C_c) was much less than the case capacitive reactance due to C_e at the three frequencies of interest. Thus C_c was neglected in the stacked performance analysis. The approximate equivalent circuit for analysis purposes is shown in Fig. 20*. The interconnecting transmission line is of length $B\ell$ and characteristic impedance Zo. The transmission line parameters depend on the circuit in which the package is imbedded. For the diode in series with a coaxial line of .2850 inches diameter, the interconnecting transmission line has $Zo \approx 76\Omega$ and electrical length of .040 inches. The problem was programmed on a digital computer and the results are presented in Table V for a stack of three -3 pf devices.

TABLE V.

NORMALIZED POWER EXTRACTED AT CHIP 3

Chip No.	PS	VDS		Pp	VDP		PU	EU	
1	1.000	3.03	0.0°	1.000	1.41	0.0°	0.988	1.81	0.0°
2	1.015	3.05	0.19	0.999	1.41	0.191°	1.982	1.82	0.381°
3	1.044	3.1	0.565°	0.981	1.397	0.577°	2.981	1.82	1.41°

Normalized Power Extracted at Chip 1

Chip No.									
1	1.000	3.03	0.0°	1.000	1.41	0.0°	2.980	1.81	0.0°
2	1.015	3.05	0.196°	0.999	1.41	0.191°	1.994	1.815	0.381°
3	1.044	3.10	0.565°	0.981	1.40	0.577°	1.000	1.82	1.41°

* This stacking analysis accounts for first order effects. A more complete analysis is easily accomplished using loop or modal circuit analysis. The above analysis technique was chosen because of the physical insight it provides.

The pump and signal frequency input power was applied at chip 3 and normalized to chip 1 in both cases. For three chips one would expect three times the power of each chip for the stack. The electrical phase difference between the chips, however, results in their not being in exact series (exact phase) hence the power delivered at the USB is 1% less than (99% stacking efficiency) that of an exact series stack. These numbers are functions of the transmission lines between the chips whose properties are affected by the circuit environment. For example, a lower characteristic impedance results in worsened phase conditions and less normalized available power. Care must be taken in the design of the circuit in which the diode is embedded to insure good stacking efficiency.

Similar results were obtained for the two chip stacked varactor.

C. High Power Upconverter Performance

Some two stack and three stack diodes were procured. Both had C_j min $\approx$ 1 pf but the 2x had package higher efficiency chips than the 3x package. Thus each stack will be compared with its equivalent single chip packaged diode for efficiency and output power. Power dissipation capabilities of the packages will also be examined.

A 2x package was soldered into the single chip circuit. This package contained two chips of the type used in Section IV. Analog power curves of the results are shown in Fig. 22. The maximum power delivered was 5.0 watts with 10 watts of pump and 2 watts of signal power. The circuit was stable as in the case of the single chip device. The pump efficiency was down some 16% from that noted in Section IV. However, the package parasitics altered the diode impedance and the circuit had to be tuned externally. This condition reduces efficiency due to the extra losses incurred in the filters when matching externally. Thus some efficiency degradation is due to the package stacking efficiency and some due to added circuit losses. Also the type of package used is of the second generation design in Fig. 21 which is different from that of Fig. 13 for which the stacking efficiency was calculated. It was anticipated that the stacking efficiency due to package changes alone would be degraded.

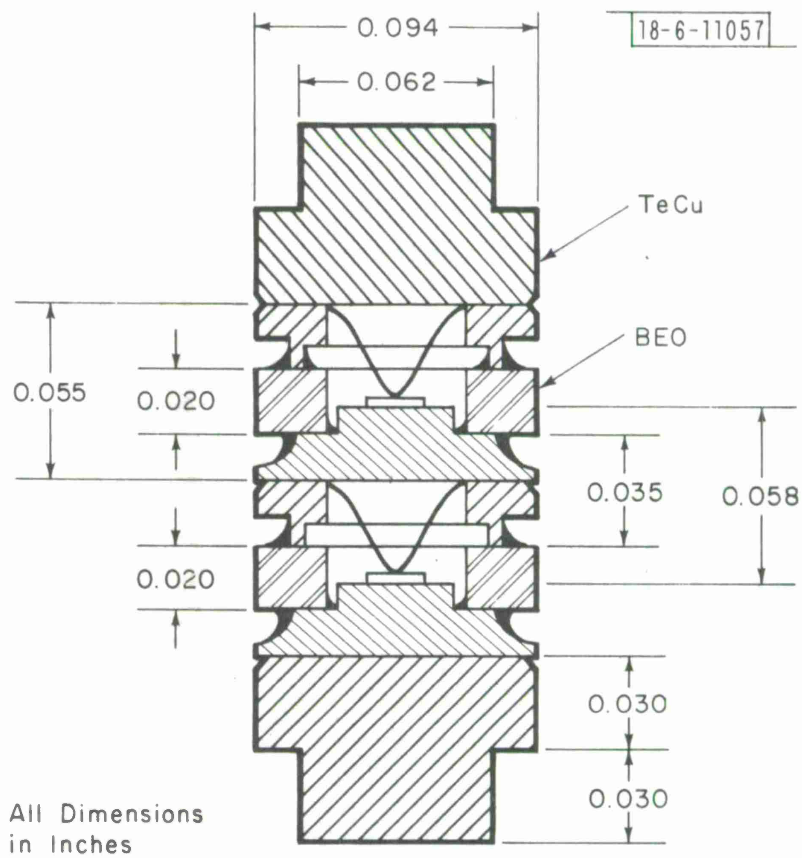

Fig. 21. Second generation stacked package.

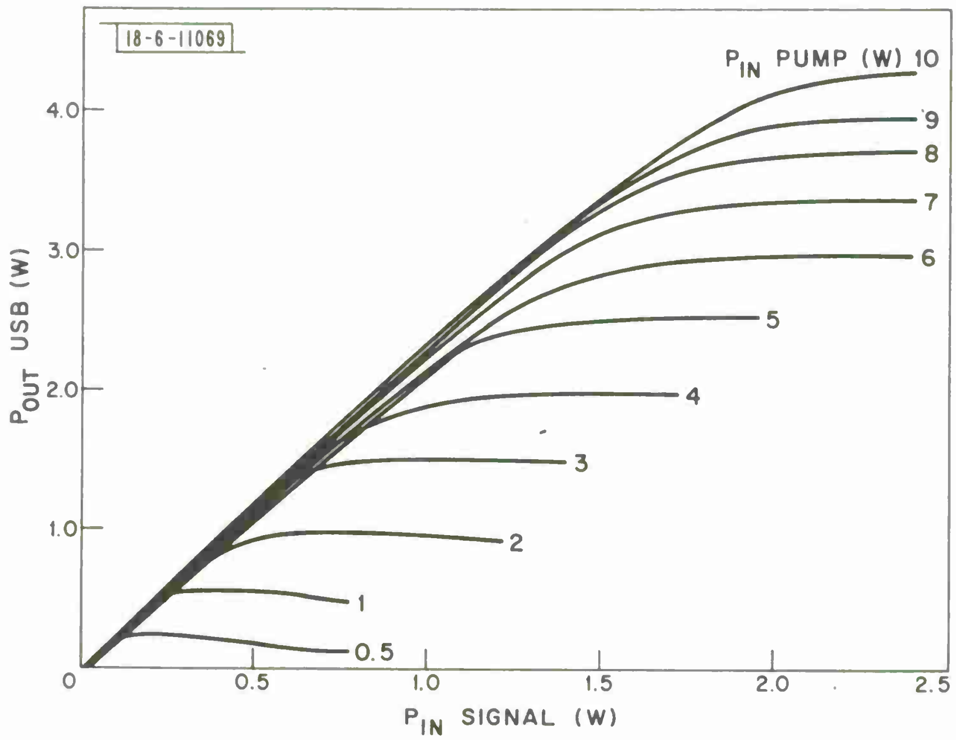

Fig. 22. Performance curves — 2x diode.

Nevertheless, the 2x package did easily deliver four times the power of the single chip device. The power limitation appeared to be thermal. Under fixed bias conditions the varactors could be driven hard enough to develop reverse bias current and operate properly until the power dissipation was great enough to burn them out. Table VI shows the results of circuit impedance measurements made on a 2x diode at the package terminals after tuning the diode at each point. A comparison with Table III shows the difference in the impedance levels. At the 10 watt pump drive level, the circuit and diode dissipated 7 watts.

A 3x diode of the lower efficiency chips was run in the same single chip circuit. This package had the lower efficiency chips because they were available. Figures 23 and 24 show the results of this diode for the single and 3x stacked chips respectively. A comparison between Figs. 23 and 12 indicates the relative efficiency of the two types of chips. The efficiency of the 3x package was slightly degraded from that of the single chip package which was not alarming due to the fact that the stacked package was of the second generation design. The interesting fact is that at the 20 watt pump level, the circuit dissipated 17.8 watts. The aluminum circuit block heated somewhat but the important thing is that the diode did continue to operate.

A 3x diode of the high efficiency chips should easily deliver 10 watts without thermal problems.

Impedance measurements were made on the circuit with the diodes removed using the techniques of Section IV. The diode impedances and circuit efficiency versus power level are given in Table VII.

The impedance levels of the stacked varactor package were markedly different particularly at the x-band frequencies from those measured on the single chip package. The problem of characterizing package parasitics is more complicated for stacked varactors than that presented in the appendix for the pill prong single chip package.

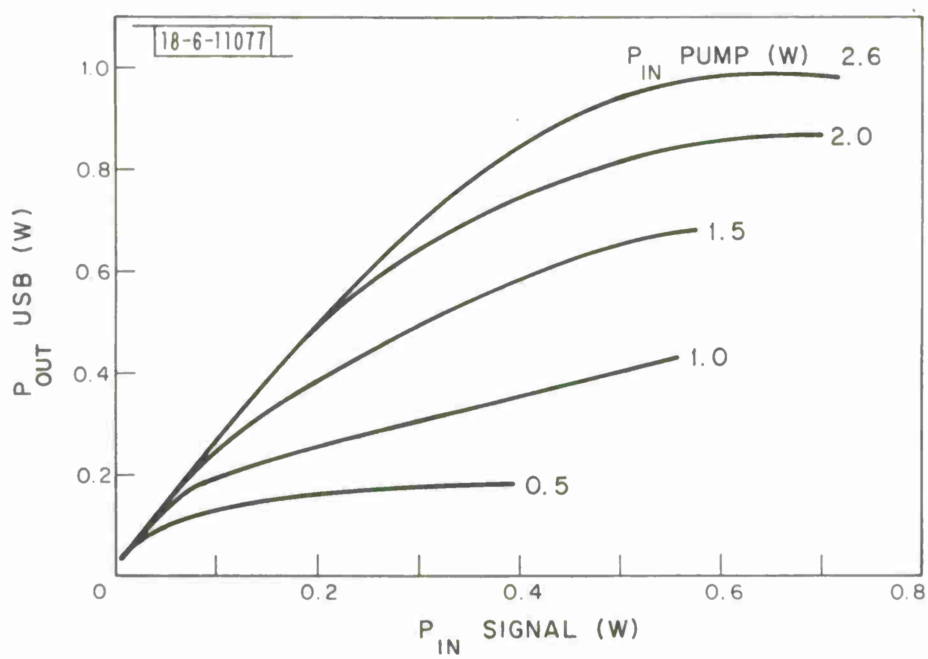

Fig. 23. Performance curves – 1x lower efficency diode.

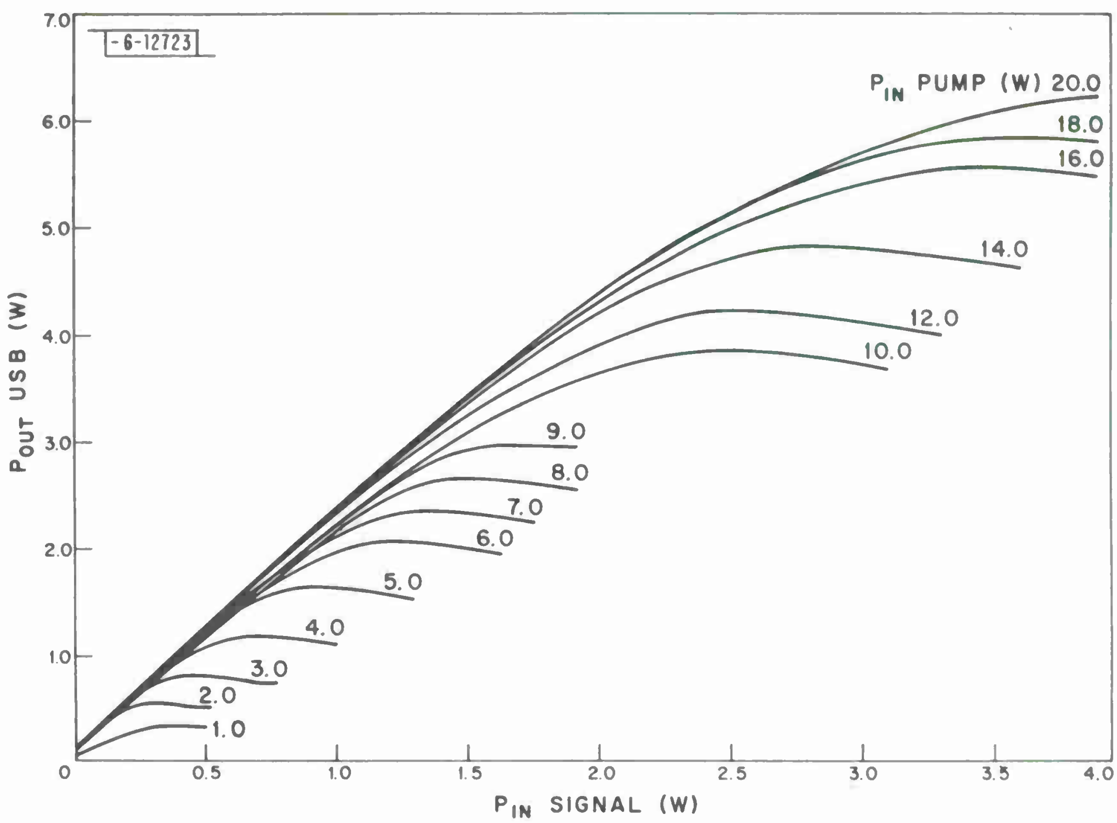

Fig. 24. Performance curves – 3x lower efficency diode.

TABLE VI

SP-2x PACKAGED DIODE IMPEDANCES

P_{OUT}(USB)	P_{PUMP}	P_{SIGNAL}	n_p	n_t	Z_s		Z_p		Z_u	
					R_s	X_s	R_p	X_p	R_u	X_u
.420 w	1.0 w	0.365 w	42%	31%	24.8	−j38.5	7.46	+j55.4	17.9	+j77.5
.880	2.0	0.620	44	33.5	23.0	−j39.4	8.35	+j54.4	16.9	+j80.4
1.33	3.0	0.820	44.3	34.8	24.1	−j39.6	7.58	+j56.5	16.9	+j80.4
1.75	4.0	0.980	43.8	35.1	22.9	−j39.1	8.8	+j55.2	16.3	+j78.3
2.28	5.0	1.63	45.6	34.4	22.3	−j41.7	9.1	+j55.2	18.6	+j79.8
2.65	6.0	1.88	44.2	33.6	22.8	−j42.4	9.4	+j56.1	20.7	+j78.9
3.03	7.0	1.95	43.3	33.9	23.0	−j42.4	9.4	+j56.2	21.6	+j81.0
3.35	8.0	1.96	41.9	33.6	23.0	−j39.4	8.6	+j54.3	21.0	+j78.8
3.60	9.0	2.09	40.0	32.5	23.0	−j39.4	9.5	+j56.1	19.1	+j82.0
3.90	10.0	2.30	39.0	31.7	23.0	−j39.4	10.3	+j56.0	21.0	+j83.7
4.40	12.0	2.73	36.7	29.9	23.0	−j39.7	9.3	+j55.1	22.0	+j86
5.65	20.0	3.90	28.3	21.2	24.7	−j35.4	11.6	+j50.0	26.0	+j86.8

TABLE VII

SP-3x PACKAGED DIODE IMPEDANCES

P_{out}(USB)	P_{pump}	P_{signal}	n_p	n_t	Z_s		Z_p		Z_u	
					R_s	X_s	R_p	X_p	R_u	X_u
5.9 ω	20.0 ω	3.8 ω	29.5%	24.8%	33.7	− j52.9	20.9	+ j56.9	35.7	+ j79.5
5.2		2.8	26.0	22.8	32.7	− j52.6	21.9	+ j56.3	45.2	+ j79.9
4.6		2.0	24.0	20.9	32.7	− j52.6	22.3	+ j57.2	46.0	+ j82.9
3.5		1.5	17.5	16.3	30.4	− j50.1			43.7	+ j81.7
2.5		1.0	12.5	11.9	30.5	− j50.2	16.1	+ j57.6	52.3	+ j78.2
1.3		0.5	6.5	6.4	30.3	− j48.1	19.0	+ j57.6	58.5	+ j83.4
5.1	16.0 ω	3.5	31.9	26.2	31.1	− j51.5	21.6	+ j56.5	49.1	+ j74.5
4.9		2.8	30.7	26.1	31.1	− j51.5	22.14	+ j56.2	46.9	+ j73.8
4.1		2.0	25.6	22.8	31.5	− j52.1	23.1	+ j54.6	42.2	+ j79.6
3.3		1.5	20.6	18.9	32.5	− j52.8	18.8	+ j56.6	61.4	+ j83.8
2.4		1.0	15.0	14.1	31.3	− j52.0	19.6	+ j57.4	64.7	+ j74.3
4.0	12.0	2.5	33.3	27.6	31.5	− j52.0	25.5	+ j52.2	38.1	+ j83.7
3.6		2.0	30.0	25.7	31.1	− j51.3	26.6	+ j53.7	42.6	+ j82.9
3.1		1.5	25.8	23.0	31.1	− j51.4	21.8	+ j51.1	40.8	+ j81.1
2.3		1.0	19.15	17.7	31.4	− j51.8	20.7	+ j59.2	56.6	+ j87.0
1.2		0.5	10.0	9.6	31.2	− j51.9	27.3	+ j54.4	61.0	+ j77.5
3.2	10.0	2.0	32.0	26.7	31.8	− j52.4	28.7	+ j55.8	41.9	+ 83.6
2.9		1.5	29.0	25.2	32.0	− j52.3	21.9	+ j50.1	38.0	+ 87.2
1.8		0.75	18.0	16.75	32.0	− j52.3	27.13	+ j53.4	40.5	+ j81.5
1.5	5.0	0.90	30.0	25.4	32.0	− j52.3	24.0	+ j54.2	32.6	+ j84.9
1.25		0.60	25.0	22.3	32.9	− j53.2	20.7	+ j49.7	40.4	+ j88.7
0.5		0.20	10.0	9.6	32.9	− j53.2	20.1	+ j50.9	51.0	+ j85.1

VI. CONCLUSIONS

Triplexer circuits can be synthesized according to the specifications given to provide efficiently matched and stable upper sideband upconverters.

There is a theoretical state-of-the-art power handling limitation for a given minimum impedance device of approximately 2.0 watts at x-band for a 5Ω impedance level. High power is achieved by stacking devices or circuits. The power goes up as N for stacked circuits and N^2 for series stacked devices given the physical limitations for efficient impedance matching. It has been shown that the use of stacked devices increases the power roughly by N^2 over the single chip, that there is no serious efficiency degradation due to small phase differences between the chip voltages and that the thermal problem is not serious for a varactor upconverter to deliver 10 watts at x-band.

Further work is required, however, on the design of stacked varactor packages to (1) minimize the phase differences between chips at high frequencies (2) ease the package parasitic problem, and (3) maintain low thermal resistances from the chip to the terminals and (4) insure good mechanical strength.

APPENDIX

A. Pill Prong Characterization

The pill prong package together with important dimensions is shown in Fig. 25. For mounting in series with a coaxial transmission line, the package can be approximated by the equivalent circuit shown in Fig. 26.

The lead inductance is due to the usually high impedance lines of short length formed by the stud and strap. The lead inductance is a function of the circuit in which the diode is imbedded, and the termination on that circuit. However, at discreet frequencies and high values of Z01 and Z02 the circuit can be approximated by the generally accepted equivalent circuit shown in Fig. 27 provided the frequency and circuit dependent parameters Ld and C_j are measured in the operating circuit at the operating frequency. For the purposes of design of the upconverter the Ld parameter was determined from small signal series resonance measurements on a diode placed in shunt with a coaxial transmission line of the size used (.2850 inches). This gave a lead inductance of 0.9 nh which is higher than the generally accepted 0.5 nh for this package. Finally the case capacitance was assumed to be the same as measured at 1 MHz; i.e., 0.16 pf. The transformation becomes

$$Z_D' = \frac{Z_D + j\omega L_D}{(1 - \omega^2 L_D C_c) + j\omega C_c Z_D} \tag{17}$$

where

Z_D' = diode impedance at the package terminals
Z_D = diode impedance
L_D = lead inductance
C_c = case capacitance

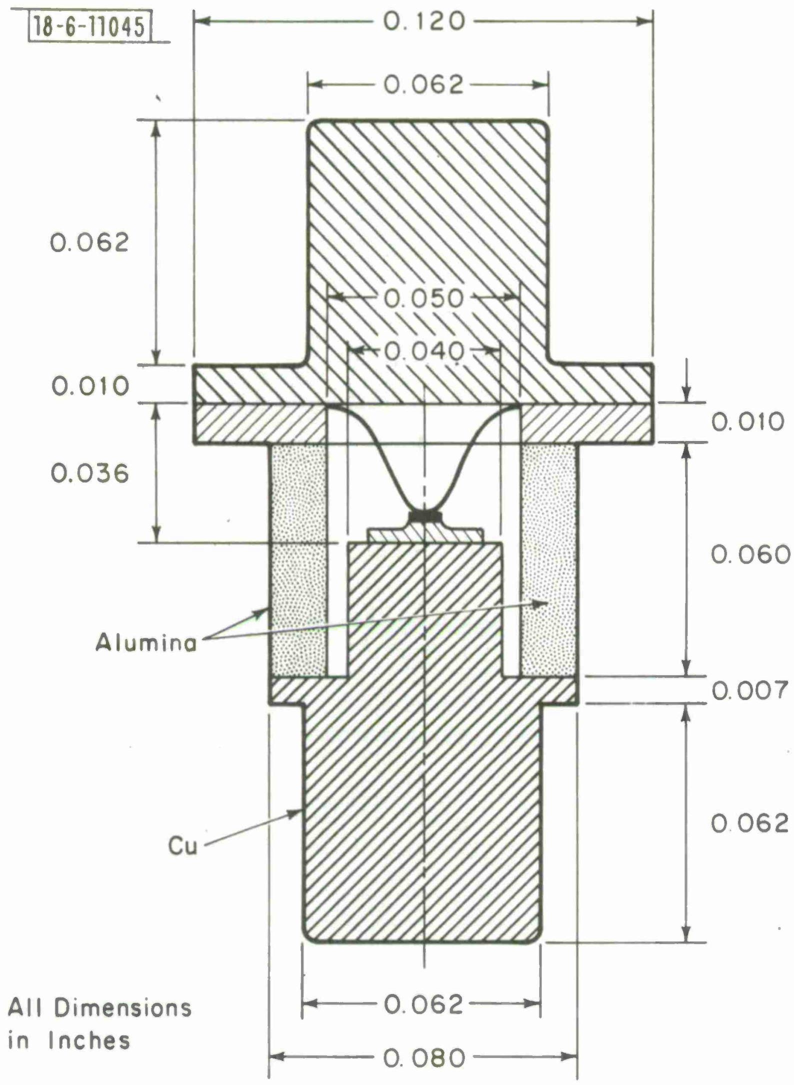

Fig. 25. Pill prong package.

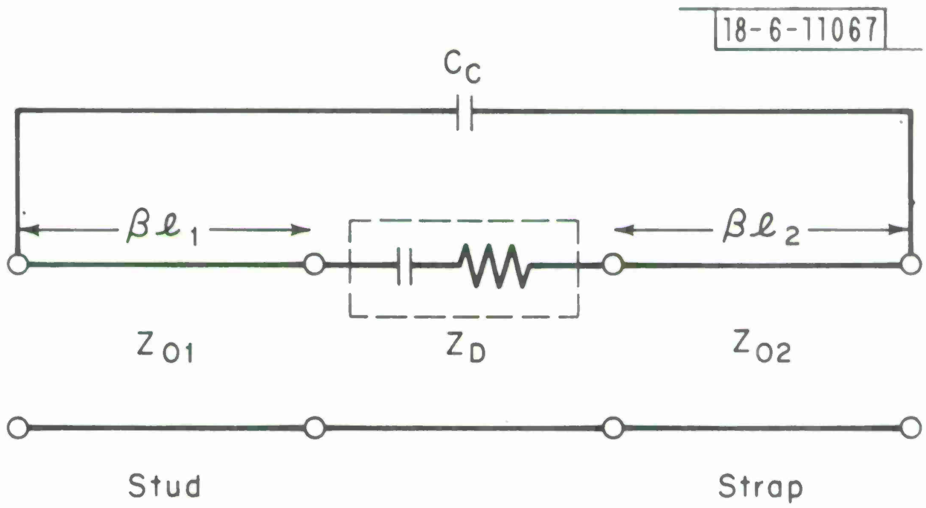

Fig. 26. Equivalent circuit pill prong package.

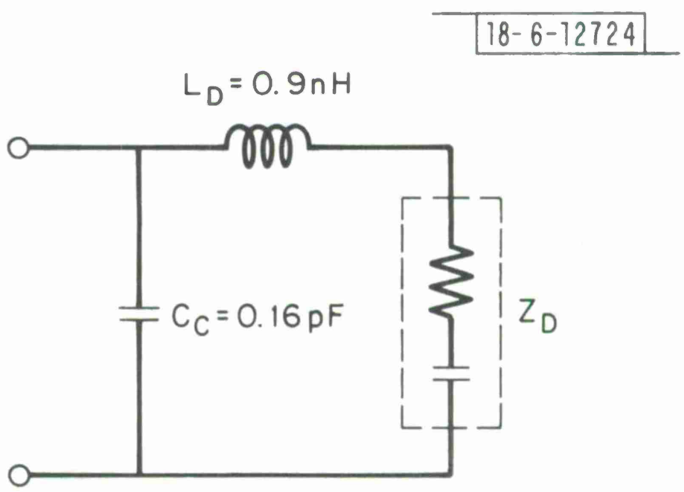

Fig. 27. Simplified equivalent circuit pill prong package.

B. Matrix Representation of Varactor Packages

The single chip package may be characterized as a general 3 port linear lossless network. Two of the ports representing the two package terminals and the third representing the chip terminals. The impedance transformation between the chip and one set of diode terminals is given by the familiar bilinear transformation whose elements are a function of the impedance presented to the other pair of package terminals. Small signal measurements at one pair of package terminals on a diode mounted in the operating circuit coupled with a knowledge of the $C_j(V)$ diode characteristics provides the required information to determine the bilinear transformation between the chip and the terminals of interest. This transformation may then be applied to transform the terminal operating impedances to the junction.

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13. ABSTRACT

This report presents a logical design procedure to build stable, efficient varactor upper sideband upconverters. It establishes general design criteria to provide (1) unconditional stability, (2) low spurious, (3) predictable diode impedance levels, and (4) predictable efficiency. A sample design is included to illustrate one means of realizing the design constraints and showing the agreement between predicted and achieved stability, impedance match, efficiency, and power output.

The second part of the report discusses means of obtaining high power operation by using multiple varactors. It is concluded that the best configuration is a series stack of varactor diodes. With allowance made for the package parasitic reactances, it is proven analytically that stacked, packaged diodes operate efficiently as an upper sideband upconverter. Finally, an example of a stacked varactor upconverter design was built and measured. The agreement between predicted and obtained results is remarkably good.

14. KEY WORDS

upconverters
varactors
X-band
circuit design
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